

ABSTRACT OF THE DISCLOSURE

There are provided a central processing unit (2), a high-speed serial communication interface circuit which can be utilized for a debugging interface, for example, a USB interface circuit (3), and an external bus interface circuit (5) which can be connected to an external memory. The USB interface circuit has a plurality of input buffers (EP 1, EP 2) therein and data can be output from one of the input buffers in parallel with an input operation to the other input buffer. In a debugging mode, the USB interface circuit receives a system program, and the system program thus received can be output from the external bus interface circuit together with a memory access control signal. When a target program is to be downloaded from a host computer into a target system, a speed of a data transfer can be increased.